

# DATA SHEET

## **PCF1172C** **3<sup>1</sup>/<sub>2</sub>-digit LCD car clock**

Product specification

1997 Apr 16

Supersedes data of September 1993

File under Integrated Circuits, IC16

## 3½-digit LCD car clock

PCF1172C

### FEATURES

- Driving standard 3½-digit LCD with AM and PM indicators
- Internal voltage regulator for 5 V LCD
- Option for external stabilized voltage supply
- 4.19 MHz oscillator
- Integrated oscillator output capacitor and polarization resistor
- Operating ambient temperature: -40 to +85 °C
- 40-lead plastic SMD, face down (VSO40).

### GENERAL DESCRIPTION

The PCF1172C is a single chip, 4.19 MHz CMOS clock circuit indicating hours and minutes. It is designed to drive a 3½-digit liquid crystal display (LCD) with AM and PM indicators.

Two external single-pole, single-throw switches will accomplish all time setting functions. The circuit is battery-operated via an internal 5 V voltage regulator or by an external stabilized voltage supply.

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF1172CT	VSO40	plastic very small outline package; 40 leads; face down <sup>(1)</sup>	SOT158-2
PCF1172CU	-	uncased chip in tray <sup>(2)</sup>	-

### Notes

1. See Fig.1 and Chapter "Package outline" for pin layout and package details.
2. See Chapter "Chip dimensions and bonding pad locations" for pad layout and package details.

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## PINNING

SYMBOL	PIN	DESCRIPTION
OSC OUT	1	oscillator output
OSC IN	2	oscillator input
S1	3	set hour
S3	4	±2 minute correction
BP	5	64 Hz backplane driver (common of LCD)
PM	6	segment output for PM annunciator
AM	7	segment output for AM annunciator
E2	8	segment driver
D2	9	segment driver
C2	10	segment driver
E3	11	segment driver
D3	12	segment driver
C3	13	segment driver
E4	14	segment driver
D4	15	segment driver
C4	16	segment driver
B4	17	segment driver
S2	18	set minutes
S4	19	internal voltage regulation
V <sub>SS</sub>	20	negative supply
S6	21	selectable correction mode
n.c.	22	not connected
V <sub>DD</sub>	23	positive supply
A4	24	segment driver
F4	25	segment driver
G4	26	segment driver
B3	27	segment driver
A3	28	segment driver
F3	29	segment driver
G3	30	segment driver
P1, P2	31	colon flashing
P3, P4	32	colon static
B2	33	segment driver
A2	34	segment driver
F2	35	segment driver
G2	36	segment driver
B1, C1	37	segment driver

SYMBOL	PIN	DESCRIPTION
TR	38	test reset; connect to (V <sub>DD</sub> )
TS	39	test speed-up; connect to (V <sub>DD</sub> )
(V <sub>DD</sub> )	40	positive supply for test and oscillator inputs

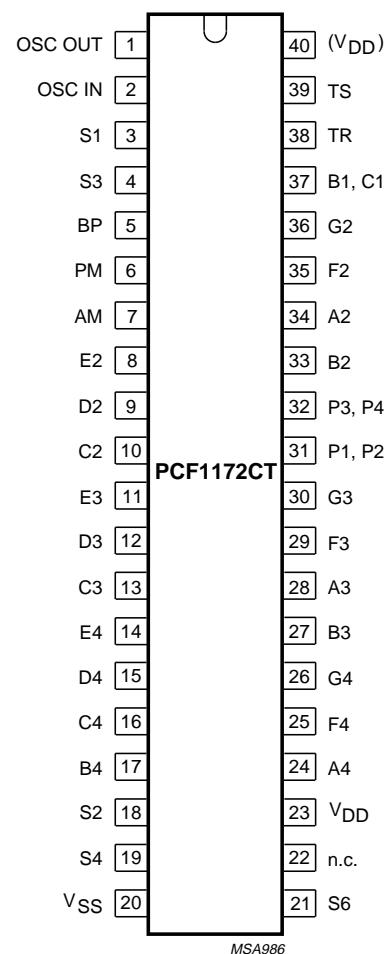


Fig.1 Pin configuration, PCF1172CT, (VSO40).

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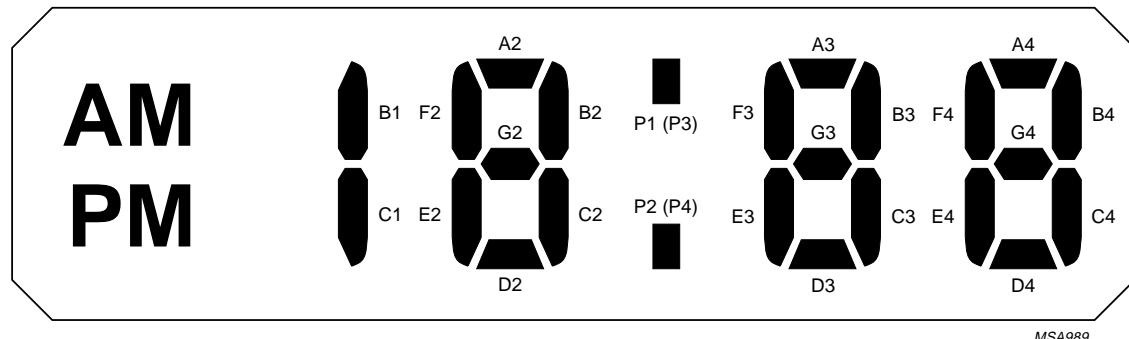


Fig.2 Segment designation of LCD.

TIME

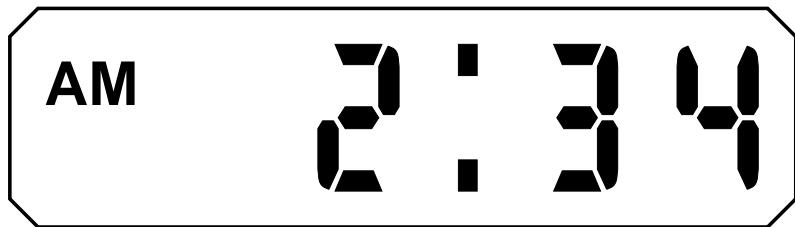


Fig.3 Display mode (12-hour with AM/PM annunciator).

**OPERATIONAL INPUTS**

Operational inputs S1, S2 and S3 have an internal pull-up resistor to facilitate use of external single-pole, single-throw switches. A specific debounce circuit is integrated as protection against contact debounce and parasitic voltages.

In the description below, an arrangement as shown in Fig.5 is assumed and S1, S2 and S3 refer to the external switches rather than the corresponding inputs.

**Set hours, switch S1**

Closure of S1 increments the hours according to the correction mode selected by S6 (see Chapter "Input options").

**Set minutes/reset seconds, switch S2**

When S2 is closed, the minute setting is corrected according to the correction mode determined by S6 (see Chapter "Input options").

The seconds counter is reset to zero each time S2 is closed, and begins running each time S2 is opened.

**Segment test/reset, switches S1 and S2**

If S1 and S2 are closed simultaneously all LCD segments are switched on. When the switches are released, the clock starts at 1 : 00.

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**Time correction ±2 minutes, switch S3**

This switch operates in two ranges:

- Displayed time  $\geq$  58 minutes 00 seconds
- Displayed time  $\leq$  1 minute 59 seconds.

When switch S3 is pressed in these ranges, the minutes and seconds are reset to zero. For displayed time  $\geq$  58 minutes 00 seconds, the hour is also incremented by one.

**INPUT OPTIONS**

In the description below S4 and S6 refer to the external switches shown in Fig.5 rather than to the corresponding inputs.

In a real application, these inputs will normally be bonded to the appropriate level to give the required function mode.

**Internal/external regulation, switch S4**

For internal regulation, S4 is closed, the internal voltage regulator is active and the voltage supply for the LCD is regulated to 5 V. For external regulation, S4 is open and the circuit has to be supplied with an externally regulated voltage.

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DD}$	supply voltage with respect to $V_{SS}$ with internal regulation disconnected	note 1	–	8	V
$V_I$	all input voltages		$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
$T_{amb}$	operating ambient temperature		–40	+85	°C
$T_{stg}$	storage temperature		–55	+125	°C

**Note**

1. Connecting the supply voltage with reverse polarity, will not harm the circuit, provided the current is limited to 10 mA by the external resistor.

**HANDLING**

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advisable to take handling precautions appropriate to handling MOS devices. Advice can be found in "Data Handbook IC16, General, Handling MOS Devices".

**Single/continuous correction mode, switch S6**

For single-set correction mode, S6 is connected to  $V_{DD}$ . Each closure of S1 or S2 advances the counter by one.

For continuous-set correction mode, S6 is connected to  $V_{SS}$ . Momentary closure of S1 or S2 causes single increments as for single-set correction mode. If S1 or S2 is kept closed for more than 1s, the counter is automatically incremented by 1 for each full second that S1 or S2 is kept closed.

**TESTING**

In normal operation the test inputs TR (pin 38) and TS (pin 39) have to be connected to  $V_{DD}$  (pin 23). A test frequency (64 Hz) is available at BP (pin 5). The test mode is activated by connecting TS to  $V_{SS}$  (pin 20). All output frequencies are then increased by a factor of 65536. In this mode the maximum input frequency is 100 kHz (external generator at OSC IN). By connecting TR to  $V_{SS}$  all counters (seconds, minutes and hours) are stopped. After connecting TR to  $V_{DD}$  all counters start from an initial state.

The switches/inputs described above also operate in the test mode.

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## CHARACTERISTICS

$V_{DD} = 5$  V;  $V_{SS} = 0$  V;  $T_{amb} = -40$  to  $+85$  °C; crystal:  $f = 4.194304$  MHz;  $R_s = 50$  Ω;  $C_L = 12$  pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
$V_{DD}$	supply voltage	external regulation	3	–	6	V
	external regulation		3	–	6	V
	internal regulation	$I_{REG} = 1$ mA	4	5	6	V
$I_{REG}$	regulation current with internal regulation		0.2	–	5	mA
$I_{DD}$	current consumption	all switches open; without LCD; internal regulation disconnected; note 1	50	400	700	μA
$r_o$	differential internal impedance	$I_{REG} = 1$ mA	–	–	150	Ω
<b>Oscillator (pins 1 and 2; note 2)</b>						
$t_{osc}$	start time		–	–	200	ms
$\Delta f/f_{osc}$	frequency stability	$\Delta V_{DD} = 100$ mV	–	$0.2 \times 10^{-6}$	$1 \times 10^{-6}$	
$R_{fb}$	feedback resistance		0.1	–	1	MΩ
$C_i$	input capacitance		–	–	9	pF
$C_o$	output capacitance		19	24	29	pF
<b>Switches S1, S2 and S3 (pins 18, 3 and 4)</b>						
$I_i$	input current	with inputs connected to $V_{SS}$	50	150	500	μA
$t_d$	debounce time		32	–	150	ms
$R_s$	segment driver output resistance	$I_L = \pm 50$ μA	–	1	2.5	kΩ
$R_{BP}$	backplane driver output resistance	$I_L = \pm 250$ μA	–	0.2	0.5	kΩ
$f_{BP}$	backplane driver output frequency		–	64	–	Hz
$V_{offset(DC)}$	LCD DC offset voltage	$R_L = 200$ kΩ; $C_L = 1$ nF	–	–	±50	mV

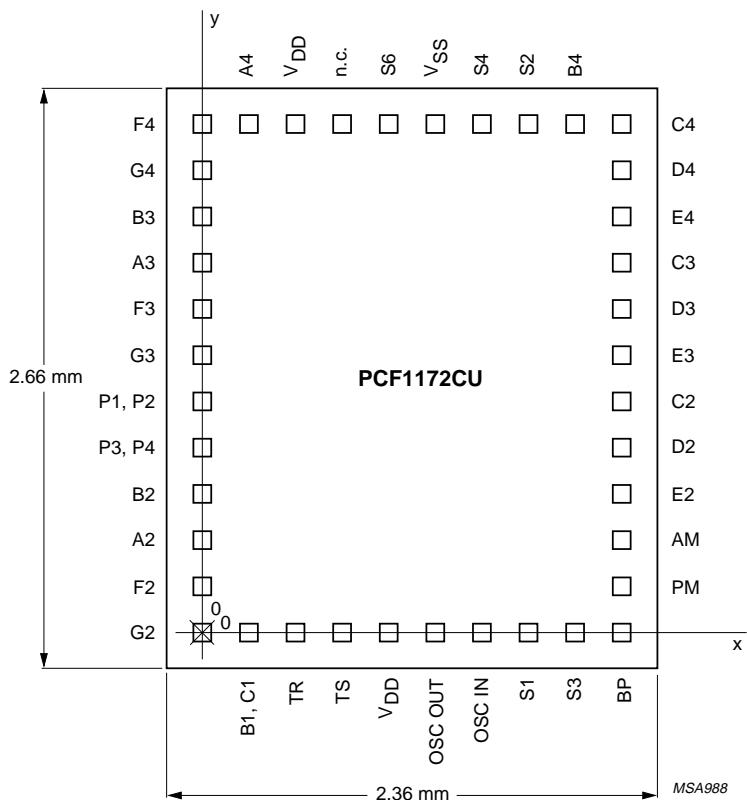
## Notes

1. The current  $I_{EXT} = I_{REG} + I_{DD} + 2 \times I_i$  (+ LCD current).
2. For correct operation of the oscillator:  $V_{DD} \geq 3$  V.

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## CHIP DIMENSIONS AND BONDING PAD LOCATIONS



n.c. = not connected.

Chip area: 6.28 mm<sup>2</sup>.

Bonding pad dimensions: 110 µm × 110 µm.

Chip thickness: 381 ±25 µm.

Fig.4 Bonding pad locations, PCF1172CU; 40 terminals.

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**Table 1** Bonding pad locations (dimensions in  $\mu\text{m}$ )

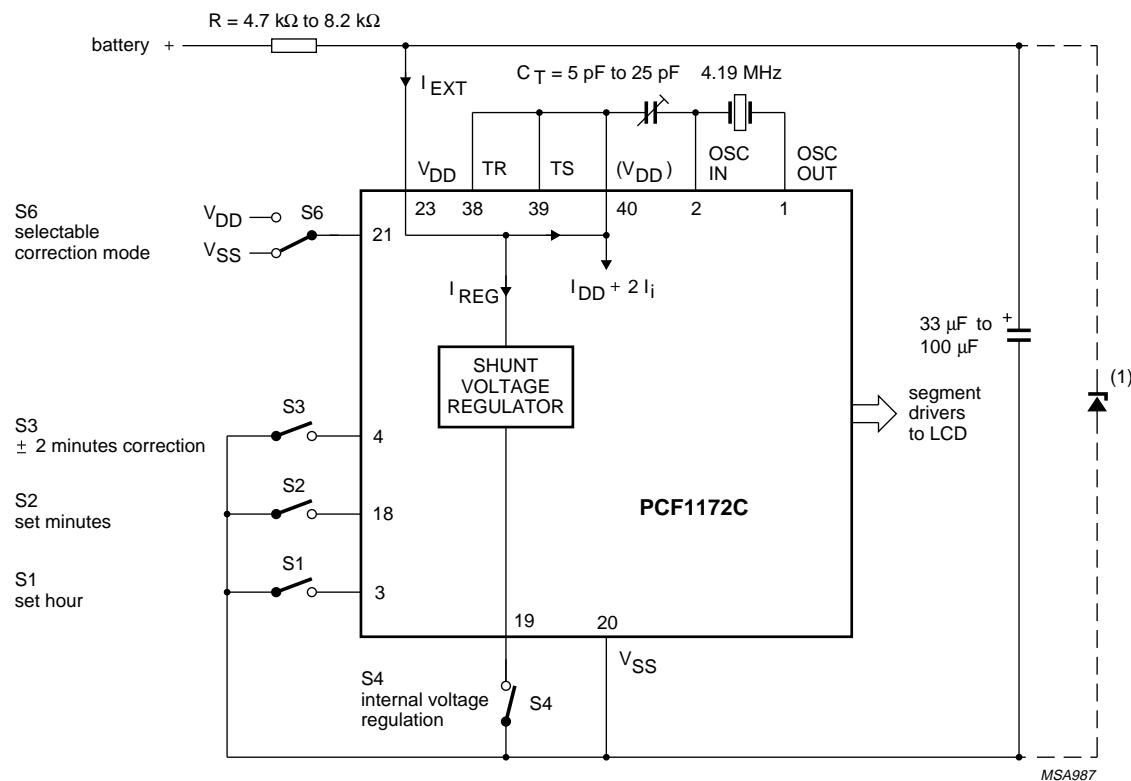
All x/y coordinates are referenced to the pad G2, see Fig.4.

PAD	x	y	PAD	x	y
OSC OUT	1060	0	S6	860	2320
OSC IN	1260	0	n.c.	660	2320
S1	1460	0	V <sub>DD</sub>	460	2320
S3	1680	0	A4	240	2320
BP	1920	0	F4	0	2320
PM	1920	240	G4	0	2080
AM	1920	460	B3	0	1860
E2	1920	660	A3	0	1660
D2	1920	860	F3	0	1460
C2	1920	1060	G3	0	1260
E3	1920	1260	P1, P2	0	1060
D3	1920	1460	P3, P4	0	860
C3	1920	1660	B2	0	660
E4	1920	1860	A2	0	460
D4	1920	2080	F2	0	240
C4	1920	2320	G2	0	0
B4	1680	2320	B1, C1	240	0
S2	1460	2320	TR	460	0
S4	1260	2320	TS	660	0
V <sub>SS</sub>	1060	2320	V <sub>DD</sub>	860	0
chip corner (max. value)	-220	-170			

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## APPLICATION INFORMATION



(1) Only required if internal regulation is disconnected.

From pin 2 (OSC IN) to any other pin the stray capacitance should not exceed 2 pF.

Fig.5 Typical application diagram.

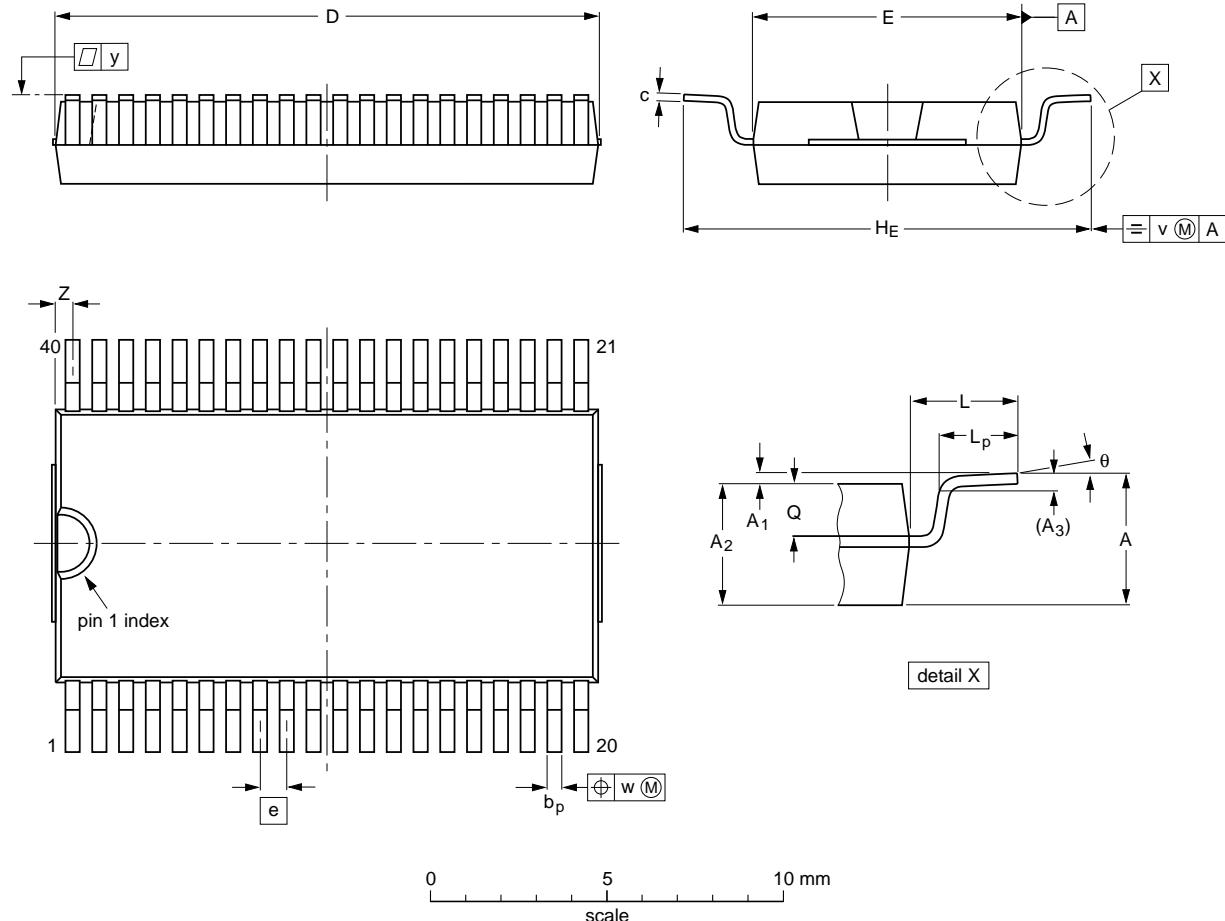
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## PACKAGE OUTLINE

VSO40: plastic very small outline package; 40 leads; face down

SOT158-2



## DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.70 0.1	0.3 0.1	2.45 2.25	0.25	0.42 0.30	0.22 0.14	15.6 15.2	7.6 7.5	0.762	12.3 11.8	2.25	1.7 1.5	1.15 1.05	0.2	0.1	0.1	0.6 0.3	7° 0°
inches	0.11 0.004	0.012 0.089	0.096 0.089	0.010	0.017 0.012	0.0087 0.0055	0.61 0.60	0.30 0.29	0.03	0.48 0.46	0.089	0.067 0.059	0.045 0.041	0.008	0.004	0.004	0.024 0.012	0° 0°

## Note

1. Plastic or metal protrusions of 0.4 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT158-2					92-11-17 95-01-24

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### SOLDERING

#### Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

#### Reflow soldering

Reflow soldering techniques are suitable for all VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

#### Wave soldering

Wave soldering techniques can be used for all VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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### DEFINITIONS

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**NOTES**

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